

What is claimed:

- 1 1. A method for manufacturing a semiconductor device, the method comprising
2 the steps of:
3 (a) forming a gate dielectric layer on a semiconductor layer;
4 (b) forming a first conduction layer having a specified pattern on the gate dielectric
5 layer;
6 (c) forming sidewall insulation layers on side walls of the first conduction layer;
7 (d) forming a source region and a drain region in the semiconductor layer;
8 (e) depositing a first insulation layer that covers the first conduction layer and the
9 sidewall insulation layers, the first insulation layer comprising a material different from that
10 of the sidewall insulation layers;
11 (f) planarizing the first insulation layer until an upper surface of the first conduction
12 layer is exposed;
13 (g) removing a part of the first conduction layer in a manner that the gate dielectric
14 layer is not exposed to thereby form a recessed section on the first conduction layer between
15 the sidewall insulation layers;
16 (h) partially filling a second conduction layer in the recessed section to form a gate
17 electrode that includes at least the first conduction layer and the second conduction layer;
18 (i) forming a second insulation layer at the recessed section on the second conduction
19 layer, the second insulation layer being composed of a material different from that of the
20 first insulation layer;
21 (j) etching the first insulation layer to form a first through hole that reaches the
22 source region or the drain region; and
23 (k) forming a first contact layer in the first through hole.

- 1 2. A method for manufacturing a semiconductor device according to claim 1,
2 wherein, in the step (j), the second insulation layer and the sidewall insulation layers are
3 composed of a material that is more difficult to etch than the first insulation layer.

1 3. A method for manufacturing a semiconductor device according to claim 1,
2 wherein the first conduction layer is a silicon layer, and the step (h) includes the steps of
3 (h - 1) depositing a metal layer for siliciding the first conduction layer on the first
4 conduction layer; and
5 (h - 2) siliciding the first conduction layer to form a silicide layer.

1 4. A method for manufacturing a semiconductor device according to claim 1,
2 further comprising:

3 (l) forming a third insulation layer on the first insulation layer and the second
4 insulation layer;

5 (m) etching the third insulation layer to form a second through hole; and

6 (n) forming a second contact layer in the second through hole, wherein the first
7 through hole is continuous to the second through hole.

1 5. A method for manufacturing a semiconductor device according to claim 1,
2 wherein, in the step (j), the second insulation layer is formed from a material having a ratio
3 of an etching rate of the second insulation layer with respect to an etching rate of the first
4 insulation layer being two or greater.

1 6. A method for manufacturing a semiconductor device according to claim 1,
2 wherein the first insulation layer comprises silicon oxide and the second insulation layer
3 comprises silicon nitride.

1 7. A method for manufacturing a semiconductor device according to claim 1,
2 wherein, in the step (j), the sidewall insulation layers are formed from a material having a
3 ratio of an etching rate of the sidewall insulation layers with respect to an etching rate of the
4 first insulation layer being two or greater.

1 8. A method for manufacturing a semiconductor device according to claim 1,
2 wherein the first insulation layer comprises silicon oxide and the sidewall insulation layers
3 comprise silicon nitride.

1 9. A method for manufacturing a semiconductor device, comprising:
2 forming a gate dielectric layer on a semiconductor layer;
3 forming a first conduction layer having a specified pattern on the gate dielectric
4 layer;
5 forming sidewall insulation layers on side walls of the first conduction layer;
6 forming a source region and a drain region in the semiconductor layer;
7 removing a part of the first conduction layer in a manner so that the gate dielectric
8 layer is not exposed, to thereby form a recessed section on the first conduction layer
9 between the sidewall insulation layers, wherein the removing a part of the first conduction
10 layer is carried out after formation of the source region and the drain region;
11 forming a second conduction layer in a portion of the recessed section; and
12 forming an insulation layer in the recessed section on the second conduction layer.

1 10. A method for manufacturing a semiconductor device according to claim 9,
2 further comprising, after forming the source region and the drain region and before
3 removing a part of the first conduction layer:
4 forming a first insulating layer that covers the first conduction layer, the sidewall
5 insulation layers, and the semiconductor layer; and
6 planarizing the first insulation layer so that the first conduction layer is exposed.

1 11. A method for manufacturing a semiconductor device according to claim 10,
2 further comprising, after forming the insulation layer in the recessed section above the
3 second conduction layer:

4 etching the first insulation layer to form a first through hole that reaches the source
5 region or the drain region; and
6 forming a first contact layer in the first through hole.

Sub to claim 9.
12. A method for manufacturing a semiconductor device according to claim 9,
2 wherein the second conducting layer comprises a silicide.

13. A method for manufacturing a semiconductor device according to claim 9,
2 wherein the removing a part of the first conduction layer further includes removing a greater
3 depth of the first conduction layer from a center region than from end regions adjacent to the
4 sidewall insulation layers.

14. A semiconductor device including a field effect transistor, the field effect
2 transistor including a gate dielectric layer, a gate electrode, a source region and a drain
3 region, comprising:
4 a second insulation layer formed on the gate electrode;
5 sidewall insulation layers formed on side walls of the gate electrode;
6 a first insulation layer formed on the sides of sidewall insulation layers,
7 the gate electrode including a first conduction layer and a second conduction layer,
8 the first conduction layer being formed on the gate dielectric layer,
9 the second conduction layer being formed above the first conduction layer;
10 a first through hole reaching the source region or the drain region formed in the first
11 insulation layer; and
12 a first contact layer formed in the first through hole,
13 wherein, as the thickness of the first conduction layer is compared based on a top
14 surface of the gate dielectric layer, the first conduction layer has thickness that gradually
15 becomes greater from a central section thereof toward the side walls thereof.

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1 15. A semiconductor device including a field effect transistor, the field effect
2 transistor including a gate dielectric layer, a gate electrode, a source region and a drain
3 region, comprising:
4 a second insulation layer formed on the gate electrode;
5 sidewall insulation layers formed on side walls of the gate electrode;
6 a first insulation layer formed on the sides of sidewall insulation layers,
7 the gate electrode including a first conduction layer and a second conduction layer,
8 the first conduction layer being formed on the gate dielectric layer,
9 the second conduction layer being formed above the first conduction layer;
10 a first through hole reaching the source region or the drain region formed in the first
11 insulation layer;
12 a first contact layer formed in the first through hole,
13 wherein, as the thickness of the first conduction layer is compared based on a top
14 surface of the gate dielectric layer, an end portion of the first conduction layer has a greater
15 thickness as compared to a thickness thereof at a central section thereof.

1 16. A semiconductor device according to claim 14, wherein, as the height of an
2 upper surface of the second conduction layer is compared based on an upper surface of the
3 gate dielectric layer, the height of the upper surface of the second conduction layer gradually
4 becomes higher from a central section thereof toward the side walls.

1 17. A semiconductor device according to claim 15, wherein, as the height of an
2 upper surface of the second conduction layer is compared based on an upper surface of the
3 gate dielectric layer, the height of the upper surface of the second conduction layer at the
4 side wall sections thereof is higher than a height of the upper surface of a central section
5 thereof.

1 18. A semiconductor device according to any one of claim 15, wherein the
2 second conduction layer comprises a material selected from the group consisting of a metal,
3 a metal alloy and a metal compound.

1 19. A semiconductor device according to claim 15, wherein the first conduction
2 layer is a silicon layer, and the second conduction layer is a silicide layer.

1 20. A semiconductor device according to claim 15, further comprising:
2 a third insulation layer formed on the first insulation layer and the second insulation
3 layer;
4 a second through hole formed in the third insulation layer, being continuous with the
5 first through hole; and
6 a second contact layer formed in the second through hole.

1 21. A semiconductor device according to any one of claim 15, wherein the first
2 insulation layer is formed from silicon oxide, and the second insulation layer is formed from
3 silicon nitride.

1 22. A semiconductor device according claim 15, wherein the first insulation layer
2 is formed from silicon oxide, and the sidewall insulation layers are formed from silicon
3 nitride.

1 23. A semiconductor device according claim 15, wherein the upper surface of the
2 first insulation layer and the upper surface of the second insulation layer are substantially at
3 the same level.